1. (currently amended) A data bit counter having a width "w", comprising:

at least w_counter stages, each stage receiving at least one carry bit, and at least one count bit, each stage executing logic on the count bit and carry bit to output at least one count bit and at least one carry bit to a next highest stage, the count bits output by the stages together representing a Gray counter count value, wherein an n^{th} count bit has a value of gcount(n)' after an active clock edge associated with the counter, and the logic includes determining gcount(n)' using an XOR of a current count bit and (an output of AND of a previous count bit and a previous carry bit).

2. (currently amended) The counter of Claim 1, wherein the counter is embodied on at least one of: a field programmable gate array, and an application specific integrated circuit (ASIC).

3. (original) The counter of Claim 2, wherein the gate array is implemented in a computer device having at least a main processor and at least a communication processor communicating therewith.

4. (original) The counter of Claim 1, wherein the logic for outputting a carry bit includes determining an AND between an input carry bit and an inverted input count bit.

5. (canceled).

6. (original) The counter of Claim 4, wherein the logic includes changing a Gray code counter bit when both the previous count bit and previous carry bit have values equal to one.

7. (currently amended) The counter of Claim [[5]]1, wherein a carry bit output by a last stage establishes a carry end bit useful for resetting a most significant Gray count bit.

8. (original) The counter of Claim 7, comprising logic for executing the resetting act, the logic including determining an XOR of a current count bit with at least one other bit.

9. (currently amended) A computing device, comprising:

at least one main processor;

at least one communication processor;

at least one data buffer between the processors for transferring data there between; and

at least one Gray code counter associated with the buffer, the counter being generic in width and having a reset value that is undetermined at compilation, wherein an n^{th} count bit has a value of gcount(n)' after an active clock edge associated with the counter, and the logic includes determining gcount(n)' using an XOR of a current count bit with at least one other bit.

10. (original) The device of Claim 9, wherein the counter has a width "w" and includes at least w counter stages, each stage receiving at least one carry bit and at least one count bit, each stage executing logic on the count bit and carry bit to output at least one count bit and at least one carry bit to a next highest stage, the count bits output by the stages together representing a Gray counter count value.

11. (currently amended) The device of Claim 10, wherein the counter is embodied on at least one of: a field programmable gate array, and an application specific integrated circuit (ASIC).

12. (original) The device of Claim 10, wherein the logic for outputting a carry bit includes determining an AND between an input carry bit and an inverted input count bit.

13. (canceled).

14. (currently amended) The device of Claim [[13]] 9, wherein a carry bit output by a last stage establishes a carry end bit useful for resetting a most significant Gray count bit.

15. (original) The device of Claim 14, the counter comprising logic for executing the resetting act, the logic including determining an XOR of a current count bit with at least one other bit.

16. (currently amended) A logic device executing method acts for counting a number of bits processed, the method acts comprising:

generating a carry bit chain useful for determining which, if any, higher order bits should change in a next clock cycle;

generating a count bit chain, the chains being dependent on each other; and

using the count bit chain to indicate a count of a number of bits, the device including a Gray code counter using the chains, wherein the counter has a width "w" and includes at least w counter

stages, each stage receiving at least one carry bit, at least one count bit, each stage executing logic on the data in signal, count bit, and carry bit to output at least one count bit and at least one carry bit to a next highest stage, the count bits output by the stages together representing a Gray counter count value and further wherein an n^{th} count bit has a value of gcount(n)' after an active clock edge associated with the counter, and the logic includes determining gcount(n)' using an XOR of a current count bit and (an output of AND of a previous count bit and a previous carry bit).

17. (canceled).

18. (currently amended) The device of Claim [[17]] 16, wherein the counter is embodied on at least one of: a field programmable gate array, and an application specific integrated circuit (ASIC).

19. (original) The device of Claim 18, wherein the gate array is incorporated into a device having a main processor communicating with a communication processor.

20. (currently amended) The device of Claim [[17]]16, wherein the logic for outputting a carry bit includes determining an AND between an input carry bit and an inverted input count bit.

21. (canceled).

22. (currently amended) The device of Claim [[21]]16, wherein a carry bit output by a last stage establishes a carry end bit useful for resetting a most significant Gray count bit.

23. (currently amended) The device of Claim 22, the counter comprising logic for executing the resetting act, the logic including determining an XOR of a current count bit with (an output of an AND of an inverted current carry bit and an (AND of a next lower order count bit and a previous carry bit)).